What is claimed is:

1. A mixed-mode process introducing a hard mask layer, comprising the steps of:

providing a semiconductor structure;

sequentially forming a first conductive layer, a dielectric layer, and a second conductive layer on the semiconductor structure;

forming a first stacked structure in a portion of the second conductive layer and the dielectric layer, and revealing the first conductive layer exposed by the first stacked structure;

conformably depositing a mask layer over the first conductive layer and covering the first stacked structure thereon; and

patterning the mask layer and the first conductive layer to simultaneously form a capacitor and a second stacked structure on the semiconductor structure, wherein the capacitor comprises the first stacked structure, a patterned mask layer thereon and a patterned first

conductive layer therebelow and the second stacked structure comprises a patterned first conductive layer and a patterned mask layer stacked thereabove.

2. The process as claimed in claim 1, wherein the patterned mask layer covers sidewalls of the first stacked structure.

3. The process as claimed in claim 1, wherein the first conductive layer and the second conductive layer are polysilicon.

4. The process as claimed in claim 1, wherein the dielectric layer is silicon dioxide, silicon nitride, silicon oxynitride or a high-K material.

5. The process as claimed in claim 4, wherein the high-K material is HfO_2, ZrO_2, TiO_2, Al_2O_3, or Ta_2O_5.

6. The process as claimed in claim 1, wherein the second stacked structure is a conductive wire device.

7. The process as claimed in claim 1, wherein the mask layer is made of non-resist materials different from a material of the first conductive layer.

8. The process as claimed in claim 7, wherein the mask layer is silicon nitride, silicon dioxide or silicon oxynitride.

9. The process as claimed in claim 1, further comprising the step of selectively forming a gate dielectric layer on a portion of the semiconductor structure before forming the first conductive layer on the semiconductor structure.

10. The process as claimed in claim 9, further comprising the step of patterning the gate dielectric layer formed on the semiconductor structure during patterning of the mask layer and the first conductive layer to thereby form a second stacked structure, the second stacked structure having a patterned first conductive layer, a patterned mask layer and a patterned gate dielectric layer stacked on the semiconductor structure.

11. The process as claimed in claim 10, wherein after the capacitor and the second stacked structure are

formed on the semiconductor structure, the method further comprises steps of:

forming source/drain regions in the semiconductor structure on opposite sides of the second stacked structure;

forming a spacer on sidewalls of the second stacked structure; and

selectively forming a silicide layer on top of the source/drain regions to form a MOSFET device comprising the second stacked structure on the semiconductor structure.

12. A mixed-mode process introducing a hard mask layer, comprising the steps of:

providing a semiconductor structure having a conductive region, a metal-oxide semiconductor (MOS) region and a capacitor region;

sequentially forming a first conductive layer, a dielectric layer, and a second conductive layer on the semiconductor structure;

forming a first stacked structure in a portion of the second conductive layer and the dielectric layer within the capacitor region, and revealing the first conductive layer exposed by the first stacked structure;

conformably depositing a mask layer over the first conductive layer and covering the first stacked structure thereon;

respectively forming a first pattern, a second pattern and a third pattern on the mask layer within the capacitor region, the conductive region and the MOS region, wherein the first pattern covers the mask layer over the first stacked structure and wherein the second pattern and the third pattern respectively covers other portion of the mask layer; and

patterning the mask layer and the first conductive layer to simultaneously form a capacitor, a second stacked structure and a third stacked structure on the semiconductor structure respectively within the capacitor region, the conductive region and the MOS region, wherein the capacitor comprises the first stacked structure, a

patterned mask layer thereon and a patterned first conductive layer therebelow and the second stacked structure and the third stacked structure each comprises a patterned first conductive layer and a patterned mask layer thereabove.

13. The process as claimed in claim 12, wherein the patterned mask layer covers sidewalls of the first stacked structure.

14. The process as claimed in claim 12, wherein the first conductive layer and the second conductive layer are polysilicon.

15. The process as claimed in claim 12, wherein the dielectric layer is silicon dioxide, silicon nitride, silicon oxynitride or a high-K material.

16. The process as claimed in claim 15, wherein the high-K material is HfO_2, ZrO_2, TiO_2, Al_2O_3, or Ta_2O_5.

17. The process as claimed in claim 12, wherein the second stacked structure is a conductive wire device.

18. The process as claimed in claim 12, wherein the mask layer is a non-resist material different from a material of the first conductive layer.

19. The process as claimed in claim 18, wherein the mask layer is silicon nitride, silicon dioxide or silicon oxynitride.

20. The process as claimed in claim 12, further comprising the step of selectively forming a gate dielectric layer on a portion of the semiconductor structure within the MOS region before forming the first conductive layer on the semiconductor structure.

21. The process as claimed in claim 20, further comprising the step of patterning the gate dielectric layer formed on the semiconductor structure within the MOS region during patterning of the mask layer and the first conductive layer to thereby form a third stacked structure comprising a patterned first conductive layer, a patterned mask layer and a patterned gate dielectric layer stacked on the semiconductor structure.

22. The process as claimed in claim 21, wherein after the capacitor, the second stacked structure and the third stacked structure are formed on the semiconductor structure, the method further comprises the steps of:

forming source/drain regions in the semiconductor structure on opposite sides of the third stacked structure within the MOS region;

forming a spacer on sidewalls of the third stacked structure; and

selectively forming a silicide layer on top of the source/drain regions to form a MOSFET device comprising the third stacked structure on the semiconductor structure.